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10/575,819	04/13/2006	Seong-Young Lee	PANK01867 US	5258

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/575,819	LEE ET AL.	
	Examiner	Art Unit	
	SARAH K. SALERNO	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16-22 and 24-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,16-22 and 24-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 6 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US PGPub 2005/0110924)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Claim 1: Kim teaches a thin film transistor comprising:

a gate electrode (124); a gate insulating layer (140) formed on the gate electrode; a semiconductor layer (154) formed on the gate insulating layer and disposed opposite the gate electrode; a source electrode (173) and a drain electrode (175) that are formed at least in part on the semiconductor layer and face each other;

a passivation layer (180) formed on the source electrode, the drain electrode, and a portion of the semiconductor layer that is not covered with the source electrode and the drain electrode; and

a shielding electrode (88) formed on the passivation layer and disposed on a region between the source electrode and the drain electrode, wherein the shielding electrode overlaps the gate electrode, wherein the shielding electrode provides a common voltage shielding for the region on which it is disposed, and wherein the shielding electrode comprises a transparent electrode [0079] (Fig. 4).

Claim 3: Kim teaches a shielding electrode is supplied with a predetermined voltage [0086].

Claim 6: Kim teaches the shielding electrode comprises IZO or ITO [0079].

Claim 8: Kim teaches the passivation layer comprises an organic insulator [0010].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6, 8 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al. (US PGPub 2003/0133066) in view of Kubota (JP Pub No. 10-098190 of record).

Claim 1: Ono teaches a thin film transistor comprising:

a gate electrode (201a); a gate insulating layer (208); a semiconductor layer (PSI) and disposed opposite the gate electrode; a source electrode (SPM) and a drain electrode (DL) that are formed at least in part on the semiconductor layer and face each other;

a passivation layer (FPAS) formed on the source electrode, the drain electrode, and a portion of the semiconductor layer that is not covered with the source electrode and the drain electrode; and

a shielding electrode (CLT) formed on the passivation layer and disposed on a region between the source electrode and the drain electrode, wherein the shielding electrode overlaps the gate electrode, wherein the shielding electrode provides common voltage shielding fro the region on which it is disposed, and wherein the shielding electrode comprises a transparent electrode (FIG. 3, 19).

Ono does not teach the gate insulating layer formed on the gate electrode, a semiconductor layer formed on the gate insulating layer. Kubota teaches the gate insulating layer formed on the gate electrode and a semiconductor layer formed on the gate insulating layer and vice versa, both orientations being used for TFTs in display devices (Fig. 2 & 3). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the TFT gate orientation in relation to the semiconductor and gate insulating layers of Ono as required by the claim language for use in display device TFTs as taught by Kubota (Fig. 2 & 3)

Claim 2: Kubota teaches the shielding electrode is electrically isolated (FIG. 2)

Claim 3: Ono teaches a shielding electrode is supplied with a predetermined voltage [0106, 0154, and 0198].

Claim 4: Kubota teaches the predetermined voltage supplied to the shielding electrode is equal to or lower than a ground voltage (FIG. 4a-e; [0047-0051]).

Claim 5: Kubota teaches the predetermined voltage supplied to the shielding electrode is a negative voltage [0039] to prevent characteristic degradation of the image display device (Abs).

Claim 6: Kim teaches the shielding electrode comprises IZO or ITO [0079].

Claim 8: Kim teaches the passivation layer comprises an organic insulator [0010].

Claim 26: Kim teaches the shielding electrode is formed on the channel portion of the thing film (FIG. 3, 19).

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al. (US PGPub 2003/0133066) and Kubota (JP Pub No. 10-098190 of record) as applied to claim 1 above, and further in view of Hong et al. (US PGPub 2004/0066481 of record).

Regarding claim 7, as described above, Ono and Kubota substantially read on the invention as claimed, except Ono and Kubota do not teach the shielding electrode has a shape of horseshoes. Hong teaches the shielding electrode has a shape of horseshoes for use in a display device (FIG. 4a-e; [0047-0051]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made

to have modified the device taught by Ono and Kubota to have the shape of horseshoes for use in a display device as taught by Hong (FIG. 4a-e; [0047-0051]).

6. Claims 9-12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong et al. (US PGPub 2004/0066481 of record) in view of Ono et al. (US PGPub 2003/0133066).

Claim 9: Hong teaches a thin film transistor array panel comprising:

a gate line and a data tie line;

a first thin film transistor including a control electrode, an input electrode, an output electrode, and a channel portion disposed between the input electrode and the output electrode and generating a gate signal to be applied to the gate line;

a second thin film transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, a drain electrode, and a channel portion disposed between the source electrode and the drain electrode and transmitting a data signal from the data line in response to the gate signal from the gate line;

a pixel electrode connected to the drain electrode to receive the data signal; and a first shielding electrode disposed on the channel portion of the first thin film transistor (FIG. 4a-e; [0047-0051]).

Hong does not teach the first shielding electrode is formed of the same layer as the pixel electrode, the shielding electrode overlaps the control electrode and wherein the shielding electrode provides a common voltage shielding for the region on which it is disposed. Ono teaches the first shielding electrode is formed of the same layer as the

pixel electrode, the shielding electrode overlaps the control electrode and wherein the shielding electrode provides a common voltage shielding for the region on which it is disposed for use in a display device (Fig. 3, 19 and 27). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Hong to have the first shielding electrode is formed of the same layer as the pixel electrode, overlaps the control electrode and provides a common voltage shielding for the region on which it is disposed for use in a display device as taught by Ono (Fig. 3, 19 and 27).

Claim 10: Hong teaches the shielding electrode is electrically isolated (FIG. 4a-e; [0047-0051]).

Claim 11: Hong teaches a shielding electrode is supplied with a predetermined voltage to prevent the accumulation of electric charge on the light-shield film (FIG. 4a-e; [0047-0051]).

Claim 12: Hong teaches the predetermined voltage supplied to the shielding electrode is equal to or lower than a ground voltage (FIG. 4a-e; [0047-0051]).

Claim 18: Hong teaches the passivation layer comprises an organic insulator (FIG. 4a-e; [0047-0051]).

7. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong et al. (US PGPub 2004/0066481 of record) in view of Ono et al. (US PGPub 2003/0133066), as applied to claim 9 above, and further in view of Kubota (JP Pub No. 10-098190 of record).

Regarding claim 13, as described above, Hong and Ono substantially read on the invention as claimed, except Hong and Ono do not teach the predetermined voltage supplied to the shielding electrode is a negative voltage to prevent characteristic degradation of the image display device. Kubota teaches the predetermined voltage supplied to the shielding electrode is a negative voltage [0039] to prevent characteristic degradation of the image display device (Abs). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Hong and Ono to have the predetermined voltage supplied to the shielding electrode is a negative voltage to prevent characteristic degradation of the image display device as taught by Kubota [0039] (Abs).

Claim 14: Kubota teaches the predetermined voltage supplied to the first shielding electrode has a magnitude for turning of the second thin film transistor [0004, 0013, 0018-0019, 0022, 0050-0059].

8. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong et al. (US PGPub 2004/0066481 of record) in view of Ono et al. (US PGPub 2003/0133066), as applied to claim 9 above, and further in view of Kubo (US Patent 6,091,467 of record)

Regarding claim 16, as described above, Hong and Ono substantially read on the invention as claimed, except Hong and Ono do not teach a second shielding electrode disposed on the channel portions of the second thin film transistor and including the same layer as the pixel electrode. Kubo teaches a second shielding

electrode disposed on the channel portions of the second thin film transistor and including the same layer as the pixel electrode (Description of the Related Art; Figs. 9-10, 12) as being known in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Hong and Ono to have a second shielding electrode disposed on the channel portions of the second thin film transistor and including the same layer as the pixel electrode as taught by Kubo to be known in the art (Description of the Related Art; Figs. 9-10, 12)

Claim 17: Kubo teaches an insulating layer disposed between the first and the second thin film transistors and the first and the second shielding electrodes (Description of the Related Art; Figs. 9-10, 12).

9. Claims 19-22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota (JP Pub No. 10-098190 of record), in view of Ono et al. (US PGPub 2003/0133066).

Claim 19: Kubota teaches a display device comprising:

a gate line (8) and a data line; a first thin film transistor (4) including a gate electrode (8), a source electrode (10) , a drain electrode (17) and a channel portion disposed between the source electrode and the drain electrode and generating a gate signal to be applied to the gate line; a second thin film transistor (4) transmitting a data signal from the data line in response to the gate signal from the gate line (FIG. 1, 5 [0032-0060]);

a pixel electrode connected to the second thin film transistor to receive the data signal; a shielding electrode (3) disposed on the channel portion between the source and the drain electrode of the first thin film transistor; and a common electrode (2) facing the pixel electrode (FIG. 1, 5 [0032-0060]),

and wherein the shielding electrode overlaps the gate electrode (Fig. 2; [0036-0038]).

Kubota does not teach a shielding electrode is formed of the same layer as the pixel electrode and wherein the shielding electrode provides common voltage shielding for the region on which it is disposed. Ono teaches a shielding electrode disposed on the channel portions of the thin film transistor and formed of the same layer as the pixel electrode and wherein the shielding electrode provides common voltage shielding for use in a display device (Fig. 3, 19 and 27). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Hong to have the shielding electrode is formed of the same layer as the pixel electrode and providing a common voltage shielding for the region on which it is disposed for use in a display device as taught by Ono (Fig. 3, 19 and 27).

Claim 20: Kubota teaches the shielding electrode faces, the common electrode (FIG. 1).

Claim 21: Kubota teaches the shielding electrode is supplied with a predetermined voltage lower than a voltage applied to the common electrode [0004, 0013, 0018-0019, 0022, 0050-0059].

Claim 22: Kubota teaches the predetermined voltage supplied to the first shielding electrode has a magnitude for turning of the second thin film transistor [0004, 0013, 0018-0019, 0022, 0050-0059].

Claim 24: Ono teaches a dielectric disposed between the shielding electrode and the common electrode (FIG. 3 & 19).

Claim 25: Ono teaches the dielectric layer comprises a liquid crystal layer (FIG. 3 & 19).

10. Claims 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota (JP Pub No. 10-098190 of record), in view of Ono et al. (US PGPub 2003/0133066).

Claim 27: Kubota teaches a thin film transistor array panel comprising:

a gate line (8) and a data line; a first thin film transistor (4) including a control electrode, an input electrode, an output electrode, and a channel portion disposed between the input electrode and the output electrode and generating a gate signal to be applied to the gate line;

a second thin film transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, a drain electrode, and a channel portion disposed between the source electrode and the drain electrode and transmitting a date signal from the data line in response to the gate signal from the gate line;

a pixel electrode connected to the drain line to receive the data signal; and

a first shielding electrode (3) disposed on the channel portion between the source electrode and drain electrode of the second thin film transistor, and wherein the shielding electrode overlaps the gate electrode (8) (FIG. 1, 5 [0032-0060]).

Kubota does not teach the second thin film transistor is formed of the same layer as the pixel electrode. Ono teaches a shielding electrode (CLT) is formed of the same layer as the pixel electrode (27) and the first shielding electrode provides a common voltage shielding for the region on which it is disposed for use in a display device (Fig. 3, 19 and 27). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Hong to have the shielding electrode is formed of the same layer as the pixel electrode and providing a common voltage shielding for the region on which it is disposed for use in a display device as taught by Ono (Fig. 3, 19 and 27).

Claim 28: Kubota teaches a second shielding electrode disposed on the channel portion between the source electrode and the drain electrode of the first thin film transistor (FIG. 1, 5 [0032-0060]). Nishida teaches the second shielding electrode of the first thin film transistor is formed of the same layer as the pixel electrode (FIG. 2; [0318]).

Claim 29: Kubota teaches the first shielding electrode is electrically isolated (FIG. 1, 5 [0032-0060]).

Claim 30: Ono teaches the first shielding electrode comprises a transparent electrode [0079].

Claim 31: Kubota teaches the first shielding electrode is supplied with a predetermined voltage (FIG. 1, 5 [0032-0060]).

Response to Arguments

11. Applicant's arguments with respect to claims 1-14, 16-22, and 24-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-R 8:00-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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